LISTING OF THE CLAIMS

This listing of claims replaces all prior versions and listing of claims in the present application:

1-11. (Canceled)

12. (Currently amended) A clock and data recovery circuit comprising:

a phase synchronization loop including an oscillator, the oscillation frequency of which is variably controlled, said phase synchronization loop performing phase-synchronization of a recovered clock signal, output from said oscillator, with an input data signal;

a discriminator circuit, responsive to a discrimination clock signal, for discriminating said input data signal and outputting the discriminated signal;

a phase detector circuit for detecting the phase difference between an output data signal, discriminated and output by said discriminator circuit, and said input data signal; and

a phase shift circuit for shifting the phase of the recovered clock signal, output from said oscillator, based on a comparison result output from said phase detector circuit, to produce the discrimination clock signal;

the discrimination clock signal, output from said phase shift circuit, being supplied as said clock signal for discrimination to said discriminator circuit,

wherein the discriminator circuit, the phase detector circuit, and the phase shift circuit comprise a feedback loop separate from the phase synchronization loop.

13. (Currently amended) A clock and data recovery circuit comprising:

a first feedback loop at least including a first phase detector circuit for detecting the phase difference between a recovered clock signal and a received data signal;

a second feedback loop including a discriminator circuit supplied with said received data signal, and a second phase detector circuit for detecting the phase difference between an output data signal, discriminated and output by said discriminator circuit, and said received data signal, the second feedback loop being separate from the first feedback loop; and

a clock recovery circuit for being controlled by said first and second feedback loops to output the recovered clock signal;

the recovered clock signal output from said clock recovery circuit being supplied as a

discrimination clock signal for discrimination by said discriminator circuit.

14. (Previously presented) The clock and data recovery circuit according to claim 13, wherein said first feedback loop includes:

a voltage-controlled oscillator circuit for varying the oscillation frequency based on an input control signal voltage, the first phase detector circuit being supplied with the recovered clock signal output from said voltage-controlled oscillator circuit and with said received data signal to detect the phase difference between the two input signals; and

a first integrator circuit for integrating an output of said first phase detector circuit and for supplying an output voltage to said voltage-controlled oscillator circuit as the input control signal voltage; and wherein

said second feedback loop includes:

a second integrator circuit for integrating an output of said second phase detector circuit; and

a phase shift circuit receiving said recovered clock signal output from said voltage-controlled oscillator circuit and an integrated output of said second integrator circuit, for shifting the phase of said recovered clock signal in accordance with the integrated output received, to output the resulting discrimination clock signal;

said discrimination clock signal, output from said phase shift circuit, being supplied to said discriminator circuit as a clock for discrimination and output as an output clock signal.

15. (Currently amended) A clock and data recovery circuit comprising:

a first feedback loop including a first phase detector circuit for detecting the phase difference between an input reference clock signal and a recovered clock signal; and

a second feedback loop including a discriminator circuit supplied with a received data signal and a second phase detector circuit for detecting the phase difference between an output data signal discriminated and output by said discriminator circuit and said received data signal, the second feedback loop being separate from the first feedback loop;

a clock for discrimination of said discriminator circuit being supplied from a clock recovery circuit controlled by said first and second feedback loops.

16. (Previously presented) The clock and data recovery circuit according to claim 15, wherein

said first feedback loop includes:

a voltage-controlled oscillator circuit for varying the oscillation frequency based on an input control signal voltage;

a first phase detector circuit receiving the recovered clock signal output from said voltage-controlled oscillator circuit and said reference clock signal to detect the phase difference therebetween, and

a first integrator circuit for integrating an output of said first phase detector circuit to supply the resulting output voltage to said voltage-controlled oscillator circuit as a control signal voltage; and wherein

said second feedback loop includes:

a discriminator circuit supplied with said received data signal;

a second phase detector circuit supplied with the output data signal output from said discriminator circuit and with said received data signal to detect the phase difference between the two signals supplied;

a second integrator circuit for integrating an output of said second phase detector circuit; and

a phase shift circuit supplied with said recovered clock signal output from said voltage-controlled oscillator circuit and with an integrated output of said second integrator circuit to phase-shift the input reference clock signal depending on the input integrated output;

a discriminator clock signal, output from said phase shift circuit, being supplied to said discriminator circuit as the clock for discrimination, and being output as an output clock signal.

17. (Previously presented) The clock and data recovery circuit according to claim 15, wherein said first phase detector circuit includes a selection circuit for selecting said received data signal or said reference clock signal, as a signal to be subjected to phase comparison with said recovered clock signal.

18. (Previously presented) The clock and data recovery circuit according to claim 17, wherein said first feedback loop includes:

a selection circuit supplied with a reference clock signal and with said received data signal to output one of the signals based on a selection control signal;

a voltage-controlled oscillator circuit for varying the oscillation frequency based on an input control signal voltage;

a first phase detector circuit supplied with the recovered clock signal output from said voltage-controlled oscillator circuit and with the signal output from said selection circuit to detect the phase difference therebetween; and

a first integrator circuit for integrating an output of said first phase detector circuit to supply the resulting output voltage as a control signal voltage to said voltage-controlled oscillator circuit; and wherein

said second feedback loop includes:

a second integrator circuit for providing an integrated output of said second phase detector circuit; and

a phase shift circuit supplied with the recovered clock signal output from said voltage-controlled oscillator circuit and with the integrated output of said second integrator circuit to shift the phase of the input clock signal in accordance with said integrated output supplied to output the resulting discrimination clock signal;

the discrimination clock signal output from said phase shift circuit being supplied to said discriminator circuit as a signal for discrimination and being output as an output clock signal.

19. (Previously presented) The clock and data recovery circuit according to claim 13, wherein the time constant of said first feedback loop is selected to be larger than the time constant of said second feedback loop.

20. (Previously presented) The clock and data recovery circuit according to claim 15, wherein the time constant of said first feedback loop is selected to be larger than the time constant of said second feedback loop.

21. (Previously presented) The clock and data recovery circuit according to claim 14, wherein the time constant of said first integrator circuit is selected to be larger than the time constant of said second integrator circuit.

22. (Previously presented) The clock and data recovery circuit according to claim 16, wherein the time constant of said first integrator circuit is selected to be larger than the time constant of said second integrator circuit.

23. (Previously presented) The clock and data recovery circuit according to claim 18, wherein the time constant of said first integrator circuit is selected to be larger than the time constant of said second integrator circuit.

24. (Previously presented) The clock and data recovery circuit according to claim 13, wherein said clock recovery circuit comprises:

a voltage-controlled oscillator circuit for outputting the recovered clock signal included in said first feedback loop, where the oscillation frequency of said voltage-controlled oscillator circuit is variably controlled based on an input control signal obtained by integrated output of said first phase detector; and

a phase shift circuit included in said second feedback loop, said phase shift circuit receiving the recovered clock signal output from said voltage-controlled oscillator circuit and an integrated output of said second integrator circuit, for shifting the phase of said recovered clock signal in accordance with the integrated output received, to output the resulting discrimination clock signal for supply to said discriminator circuit.

25. (Previously presented) The clock and data recovery circuit according to claim 15, wherein said clock recovery circuit comprises:

a voltage-controlled oscillator circuit for outputting the recovered clock signal included in said first feedback loop, where the oscillation frequency of said voltage-controlled oscillator circuit is variably controlled based on an input control signal obtained by integrated output of said first phase detector; and

a phase shift circuit included in said second feedback loop, said phase shift circuit receiving the recovered clock signal output from said voltage-controlled oscillator circuit and an integrated output of said second integrator circuit, for shifting the phase of said recovered clock signal in accordance with the integrated output received, to output the resulting discrimination clock signal for supply to said discriminator circuit.

26. (Previously presented) The clock and data recovery circuit according to claim 14, wherein said first phase detector circuit compares the phase of said received data signal supplied to a first input end thereof with that of said recovered clock signal supplied to a second input end thereof to output a comparison result at an output end thereof;

said first integrator circuit is supplied with an output signal from said first phase detector circuit to integrate the signal supplied;

said clock recovery circuit includes a voltage-controlled oscillator supplied with an output signal of said first integrator circuit at an input end thereof to change the oscillation frequency based on an output signal from said first integrator circuit to output the resulting recovered clock signal at an output end thereof;

said recovered clock signal, output from said clock recovery circuit, being fed back to a second input end of said first phase detector circuit;

said discriminator circuit is supplied with said received data signal at a data input end thereof to discriminate said received data signal based on the discrimination clock signal supplied to a clock input terminal thereof to output a data signal at an output end thereof;

said second phase detector circuit compares the phase of the output data signal supplied to a first input end thereof from said discriminator circuit with that of said received data signal supplied to a second input end thereof to output a comparison result at an output end thereof;

said second integrator circuit is supplied with an output signal from said second phase detector circuit to integrate the signal supplied; and

a phase shift circuit supplied with said recovered clock signal output from said clock recovery circuit at an input end thereof and with an output signal from said second integrator circuit at a control signal input end thereof to shift the phase of the recovered clock signal output from said clock recovery circuit, based on said output signal, to output the resulting discrimination clock signal at an output end thereof;

the discrimination clock signal output from said phase shift circuit being supplied to said discriminator circuit as said clock signal for discrimination.